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10/564,486	01/13/2006	Hyo-Kun Son	3449-0567PUS1	9185

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EXAMINER	
MIYOSHI, JESSE Y	

ART UNIT	PAPER NUMBER
2811	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

mailroom@bskb.com

Office Action Summary	Application No.	Applicant(s)	
	10/564,486	SON, HYO-KUN	
	Examiner	**Art Unit**	
	JESSE Y. MIYOSHI	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *33,34,37-44 and 47-57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *33,34,37-44 and 47-57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 38 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claim 38 is amended to state “the super lattice structure including InGaN has a thickness of 1~3000 Å”. Claim 38 is rejected as containing new matter since the super lattice structure is not described as having a total width of 1~3000 Å, instead, in paragraph 35 of the pre-grant publication of the instant application describes that each layer of the super lattice structure has a width of 1~3000 Å.

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 42-44, 47-50 and 55-57 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 42 recites at lines 8-9 “the active layer is grown at a temperature lower than the first and second temperature”. Said limitation is unclear because the temperature at which the active layer is grown is compared to temperature values that are undefined.

Claim 42 recites at lines 12-13 “the super lattice structure is grown at a second and a third temperature…”. Said limitation is unclear because it is unclear whether said super lattice structure is the same as the super lattice structure including InGaN or a completely different structure within the device.

Claim 42 recites at lines 12-13 “the super lattice structure is grown at a second …”. Said limitation is unclear because it is unclear what “a second” is referring to, the super lattice structure is grown at a second level, a second composition, a second location.

Claim 42 recites at lines 12-13 “a third temperature higher than a first temperature…”. Said limitation is unclear because “a third temperature” alone can be an infinite number of values above the value of the first temperature and is unlimited.

Claim 56 recites at lines 12-13 “the second temperature …”. Said limitation is unclear because Examiner is unsure whether Applicant is referring to “the second” as recited in claim 42 or another second temperature.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 33, 34, 37-44 and 47-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanizawa et al. (U.S. PGPub 2003/0205711; hereinafter “Tanizawa”) and Vaudo et al. (U.S. 6,440,823; hereinafter “Vaudo”).

Re claim 33: Tanizawa teaches the general laminate structure for an LED using gallium nitride based materials having a decreased number of pits and further teaches (e.g. figure 1) a light emitting diode (LED) comprising: a first gallium nitride layer (**4**); a super lattice structure (**6**) including InGaN (multi-layers film **6** in the form of a super lattice structure having first nitride semiconductor layer made of $In_kGa_{1-k}N$ and second nitride semiconductor layer $In_mGa_{1-m}N$; e.g. paragraphs 60 and 64) on the first gallium nitride layer (**4**); an active layer (**7**) on the super lattice structure (**6**) including InGaN; and a second gallium nitride layer (p-type cladding layer **8** of a single layer made of $Al_tGa_{1-t}N$ (0=<t=<1); e.g. paragraph 76) on the active layer (**7**), wherein the super lattice structure (**6**) including InGaN has a plurality of pits formed thereon (multi-layered film **6** is formed between the buffer layer **2** and active layer **7** to decrease the number of pits occurring in each nitride semiconductor layer; e.g. paragraph 64).

Tanizawa is silent as to explicitly teaching the light emitting diode wherein a non-zero number of the plurality of pits is 50 or less per area of 5μm×5μm.

Vaudo teaches generally a Gan/InGaN light emitting diode structure with reduced number of pits and further teaches (e.g. figure 8) the light emitting diode (**100**) wherein a non-zero number of the plurality of pits (base GaN has hexagonal pit density of

approximately $10^6 cm^{-2}$ and can be reduced to less than 50 pits per cm^2; e.g. column 16, lines 15-17) is 50 or less per area of 5μm×5μm. Since 25 pits per μm^2 is approximately $2x10^8$ pits per cm^2, Vaudo's pit density of less than 50 pits cm^2 meets said claim limitation because any subsequent nitride based layer will have the same, if not less, pits than the density of pits at the base GaN layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Vaudo in the device of Tanizawa and have a base GaN layer having less than 50 pits per cm^2 allowing for a high quality epitaxial growth to be attained (see column 16, lines 29-30 of Vaudo) and since it is a goal of Tanizawa to decrease the number of pits, Vaudo's teachings would allow for high quality epitaxial layers with less pits to be grown.

Re claim 34: Tanizawa teaches the LED wherein the active layer (**7**) comprises an InGaN/InGaN structure of a multi-quantum well structure (active layer **7** of the multiple quantum-well structure is made of a nitride semiconductor containing In and Ga, preferably $In_aGa_{1-a}N$ (0=<a<1); e.g. paragraph 68).

Re claim 37: Tanizawa teaches the LED wherein the super lattice structure (**6**) including InGaN includes an $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer is formed to have a super lattice structure (multi-layers film **6** having first nitride semiconductor layer made of $In_kGa_{1-k}N$ and second nitride semiconductor layer $In_mGa_{1-m}N$; e.g. paragraph 64).

Re claim 38: Tanizawa teaches the LED wherein each layer of the $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer has a thickness of 1-3000Å (multi-layered film **6** in the form of a

super lattice structure is grown to a total thickness of 640 angstroms; e.g. paragraph 98).

Re claim 39: Tanizawa teaches the LED, wherein the super lattice structure (**6**) including InGaN has a photoluminescence characteristic of a yellow band intensity/N-doped GaN intensity ratio of 0.4 or below. Since the structure recited in the prior art is substantially identical to that of the claim, claimed properties are presumed to be present. See MPEP 2112.01(i).

Re claim 40: Tanizawa teaches the LED, wherein the active layer (**7**) is directly on the super lattice structure (**6**) including InGaN.

Re claim 41: Tanizawa teaches the LED wherein the LED is blue LED (blue LED; e.g. paragraph 2).

Re claim 42: Tanizawa teaches the general laminate structure for an LED using gallium nitride based materials having a decreased number of pits and further teaches (e.g. figure 1) a method for manufacturing a light emitting device, the method comprising the steps of: forming a buffer layer (**2**); forming an N-type gallium nitride layer (**4**) on the buffer layer (**2**); forming a super lattice structure (**6**) including InGaN (multi-layers film **6** in the form of a super lattice structure having first nitride semiconductor layer made of $In_kGa_{1-k}N$ and second nitride semiconductor layer $In_mGa_{1-m}N$; e.g. paragraphs 60 and 64) on the N-type gallium nitride layer (**4**); forming an active layer (**7**) on the super lattice structure (**6**) including InGaN; and forming a P-type gallium nitride layer (p-type cladding layer of a single layer made of $Al_tGa_{1-t}N$ (0=<t=<1); e.g. paragraph 76) on the active layer (**7**), wherein the active layer (**7**) is grown at a

temperature (800˚C; e.g. paragraph 98) lower than the first and second temperatures (900˚C), wherein the super lattice structure (**6**) including InGaN has a plurality of pits formed thereon (multi-layered film **6** is formed between the buffer layer **2** and active layer **7** to decrease the number of pits occurring in each nitride semiconductor layer; e.g. paragraph 64) and, and wherein the buffer layer (**2**) is grown at a first temperature (200-800˚C; e.g. paragraph 41), and the super lattice structure (**6**) is grown at a second (800˚C; e.g. paragraph 98) and a third temperature (950˚C) higher than the first temperature (200-800˚C; e.g. paragraph 41), and the active layer (**7**) is grown at a fourth temperature higher (less than 800˚C since active layer **7** contains a higher amount of indium) than the first temperature (200-800˚C; e.g. paragraph 41) and lower than the second (800˚C; e.g. paragraph 98) and third temperature (950˚C).

Tanizawa is silent as to explicitly teaching the method for manufacturing a light emitting device wherein a non-zero number of the plurality of pits is 50 or less per area of 5μm×5μm.

Vaudo teaches generally a Gan/InGaN light emitting diode structure with reduced number of pits and further teaches (e.g. figure 8) the light emitting diode (**100**) wherein a non-zero number of the plurality of pits (base GaN has hexagonal pit density of approximately $10^6 cm^{-2}$ and can be reduced to less than 50 pits per cm^2; e.g. column 16, lines 15-17) is 50 or less per area of 5μm×5μm. Since 25 pits per μm^2 is approximately $2x10^8$ pits per cm^2, Vaudo's pit density of less than 50 pits cm^2 meets said claim limitation because any subsequent nitride based layer will have the same, if not less, pits than the density of pits at the base GaN layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Vaudo in the device of Tanizawa and have a base GaN layer having less than 50 pits per cm^2 allowing for a high quality epitaxial growth to be attained (see column 16, lines 29-30 of Vaudo) and since it is a goal of Tanizawa to decrease the number of pits, Vaudo's teachings would allow for high quality epitaxial layers with less pits to be grown.

Re claim 43: Tanizawa teaches the method wherein the active layer (**7**) is grown at 600~800 °C (800˚C; e.g. paragraph 98).

Re claim 44: Tanizawa teaches the method wherein the active layer (**7**) comprises an InGaN/InGaN structure of a multi-quantum well structure (active layer **7** of the multiple quantum-well structure is made of a nitride semiconductor containing IN and Ga, preferably $In_aGa_{1-a}N$ (0=<a<1); e.g. paragraph 68)).

Re claim 47: Tanizawa teaches the method wherein the super lattice structure (multi-layers film **6** having first nitride semiconductor layer made of $In_kGa_{1-k}N$ and second nitride semiconductor layer $In_mGa_{1-m}N$; e.g. paragraph 64) including InGaN includes an $In_xGa_{1-x}N/In_yGa_{1-y}N$ multi-layer is formed to have a super lattice structure (super lattice structure; e.g. paragraph 60).

Re claim 48: Tanizawa teaches the method wherein each layer of the super lattice structure (**6**) including InGaN has a thickness of 1-3000Å (multi layered film **6** have layers of about 40 and 20 angstroms; e.g. paragraph 98).

Re claim 49: Tanizawa teaches the device wherein the super lattice structure (**6**) including InGaN has a photoluminescence characteristic of a yellow band intensity/N-

doped GaN intensity ratio of 0.4 or below. Since the structure recited in the prior art is substantially identical to that of the claim, claimed properties are presumed to be inherent. See MPEP 2112.01(i).

Re claim 50: Tanizawa teaches the active layer (**7**) being directly formed on the super lattice structure (**6**) including InGaN.

Re claim 51: Tanizawa teaches (e.g. figure 1) a light emitting diode (LED), comprising: a substrate (**1**); a buffer layer (**2**) on the substrate (**1**); an undoped GaN layer (upper half of undoped layer **3** made of GaN; e.g. paragraph 42) on the buffer layer (**2**); an N-type GaN layer (n-type contact layer **4**; e.g. paragraph 44) directly on the undoped GaN layer (upper half of **3**); a super lattice structure (**5, 6**; multi-layers film **6** in the form of a super lattice structure having first nitride semiconductor layer made of $In_kGa_{1-k}N$ and second nitride semiconductor layer $In_mGa_{1-m}N$; e.g. paragraphs 60 and 64) including InGaN directly on the N-type GaN layer (**4**); an active layer (**7**) on the super lattice structure (**5, 6**) including InGaN; and a P-type GaN layer (p-type cladding layer **8** of a single layer made of $Al_tGa_{1-t}N$ (0=<t=<1); e.g. paragraph 76) on the active layer (**7**), wherein the super lattice structure including InGaN has a plurality of pits thereon (multi-layered film **6** is formed between the buffer layer **2** and active layer **7** to decrease the number of pits occurring in each nitride semiconductor layer; e.g. paragraph 64).

Tanizawa is silent as to explicitly teaching the light emitting diode wherein a non-zero number of the plurality of pits is 50 or less per area of 5μm×5μm.

Vaudo teaches generally a Gan/InGaN light emitting diode structure with reduced number of pits and further teaches (e.g. figure 8) the light emitting diode (**100**) wherein a non-zero number of the plurality of pits (base GaN has hexagonal pit density of approximately $10^6 cm^{-2}$ and can be reduced to less than 50 pits per cm^2; e.g. column 16, lines 15-17) is 50 or less per area of 5µm×5µm. Since 25 pits per μm^2 is approximately $2x10^8$ pits per cm^2, Vaudo's pit density of less than 50 pits cm^2 meets said claim limitation because any subsequent nitride based layer will have the same, if not less, pits than the density of pits at the base GaN layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Vaudo in the device of Tanizawa and have a base GaN layer having less than 50 pits per cm^2 allowing for a high quality epitaxial growth to be attained (see column 16, lines 29-30 of Vaudo) and since it is a goal of Tanizawa to decrease the number of pits, Vaudo's teachings would allow for high quality epitaxial layers with less pits to be grown.

Re claim 52: Tanizawa teaches the LED, further comprising: a GaN layer (lower half of **3**) between the buffer layer (**2**) and the undoped GaN layer (upper half of **3**).

Re claim 53: Tanizawa teaches the LED, wherein the undoped GaN layer (upper half of **3**) is directly formed on the GaN layer (lower half of **3**).

Re claim 54: Tanizawa teaches the LED, wherein the active layer (**7**) comprises: an InGaN/InGaN structure (active layer **7** of the multiple quantum-well structure is made of a nitride semiconductor containing In and Ga, preferably $In_aGa_{1-a}N$ (0=<a<1); e.g. paragraph 68) of a multi-quantum well structure.

Re claim 55: Tanizawa teaches the method, further comprising: forming an undoped GaN layer (**3**) on the buffer layer (**2**) before forming the N-type gallium nitride layer (**4**).

Re claim 56: Tanizawa teaches the method, wherein the undoped GaN layer (**3**) is grown at a fifth temperature (1050˚C; e.g. paragraph 93) higher than the first temperature (200-800˚C), the second temperature (800˚C), the third temperature (950˚C) and the fourth temperature (less than 800˚C).

Re claim 57: Tanizawa teaches the method, further comprising: forming a plurality of pits (pits appear on the surface of the p-type contact layer 10 are produced from pits formed in layers below it; e.g. paragraph 33) between the active layer (**7**) and the P-type gallium nitride layer (**8**).

Response to Arguments

7. Applicant's arguments with respect to claims 33, 34, 36-44, 46-54 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSE Y. MIYOSHI whose telephone number is (571)270-1629. The examiner can normally be reached on M-F 7:30AM-5:00PM EST. Alternating Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JYM

/Ori Nadav/
Primary Examiner, Art Unit 2811